

FIGURE 1

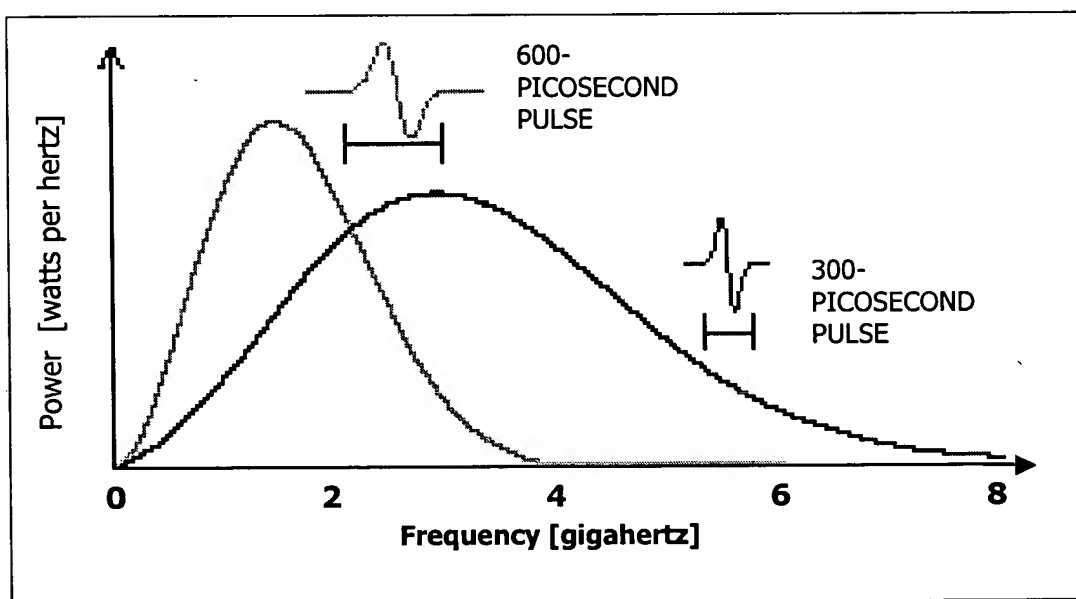
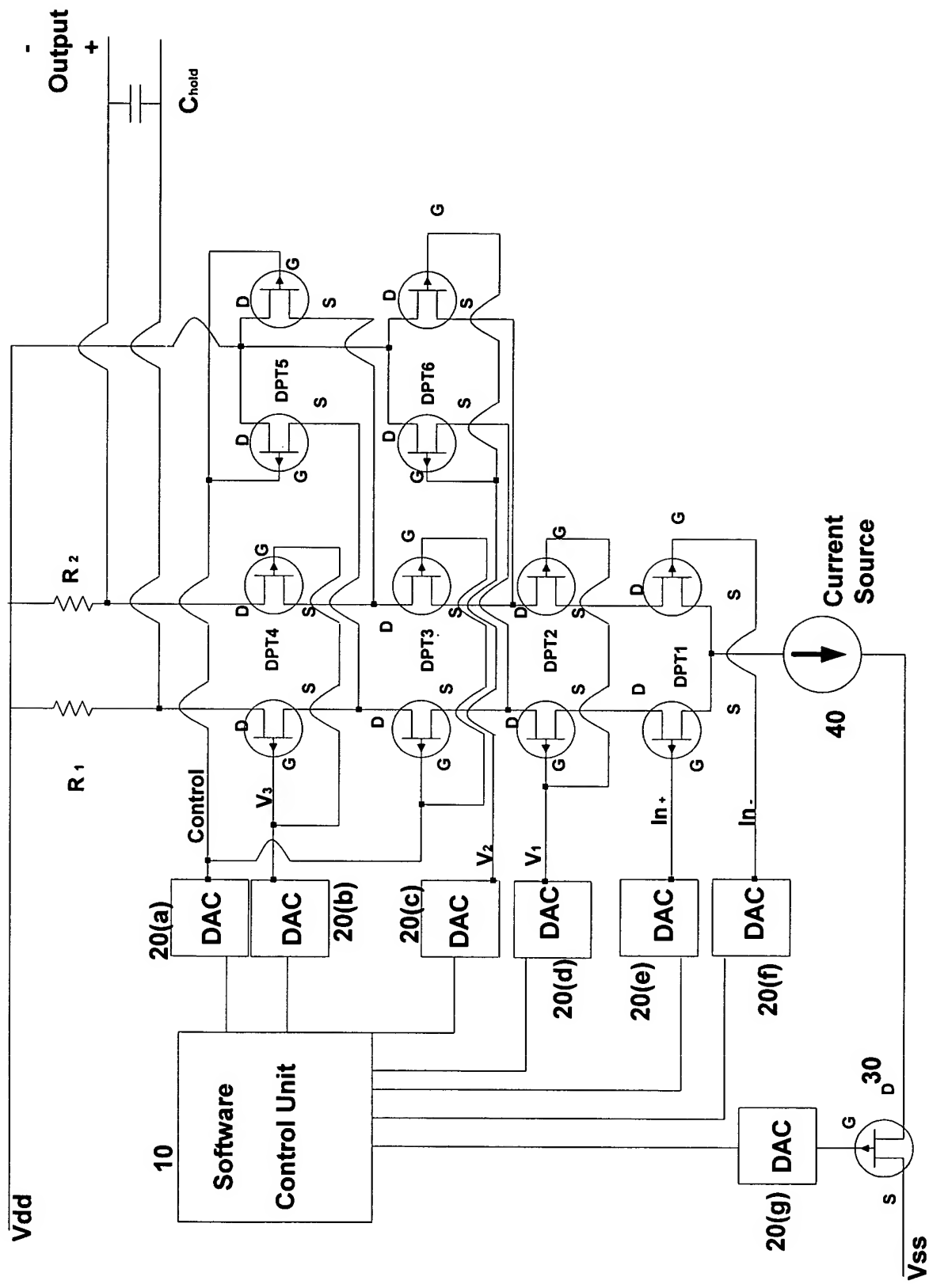
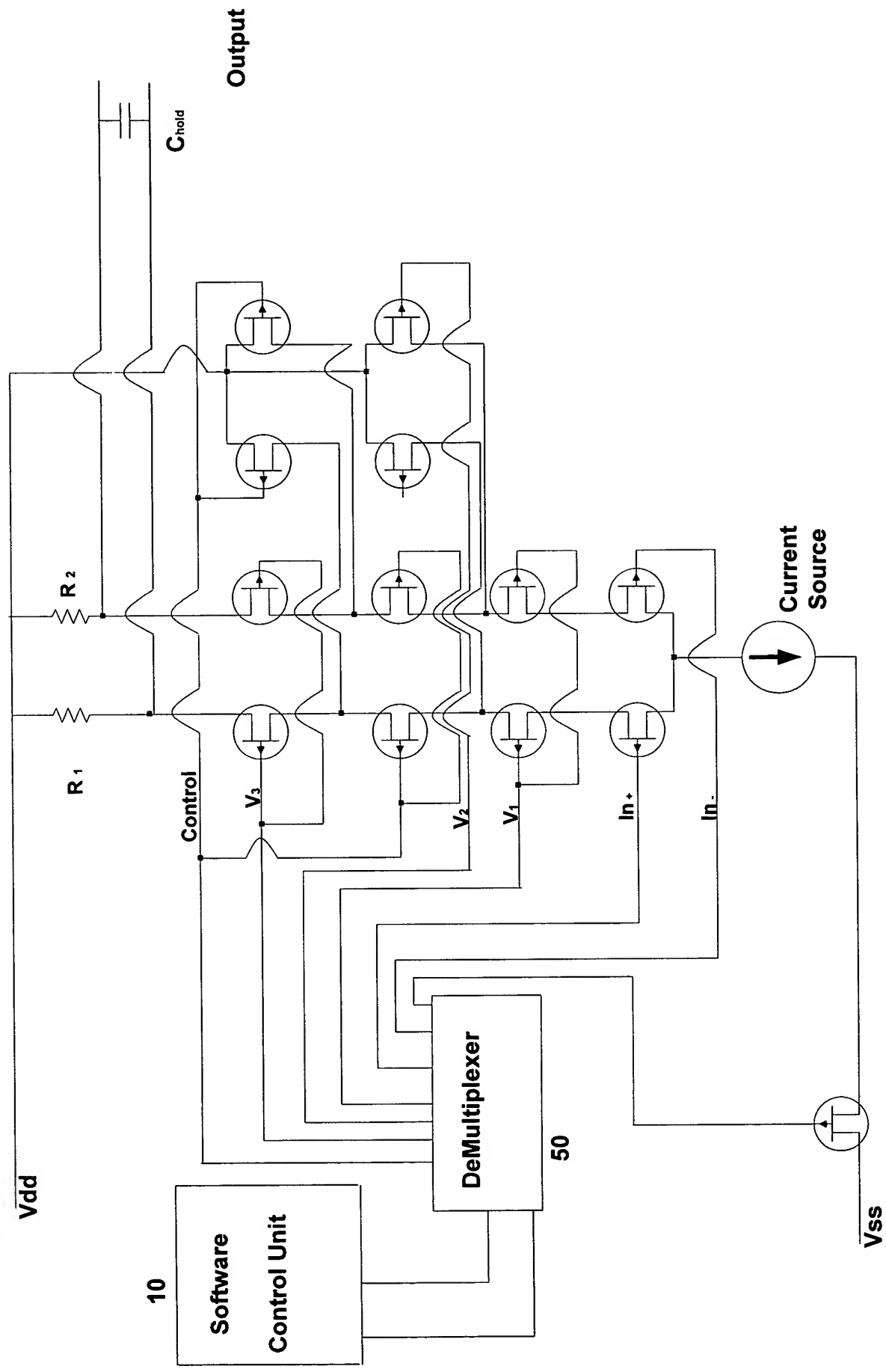


FIGURE 2

FIGURE 3



The diagram illustrates a 10-bit programmable gain amplifier (PGA) circuit. It features a 50-bit digital input bus connected to a DeMultiplexer, which provides control signals to a 10-bit digital output bus. The circuit includes a Software Control Unit, a Current Source, and a DeMultiplexer. The input stage consists of a differential pair of NMOS transistors with gates controlled by V_1 and V_2 . The sources are connected to a common source node, which is biased by a current source and a resistor R_1 . The output stage consists of a differential pair of PMOS transistors with gates controlled by V_3 and V_4 . The sources are connected to a common source node, which is biased by a current source and a resistor R_2 . The output is taken from the drains of the PMOS transistors, which are connected to a load resistor R_L and a capacitor C_{hold} . The circuit is powered by V_{dd} and V_{ss} .



The diagram illustrates a 3-stage CMOS differential amplifier. The input stage (DPT 1) is a differential pair with inputs $In +$ and $In -$, biased by a tail current source connected to Vss . The output of the first stage is connected to the gates of the second and third stages (DPT 2 and DPT 3). The second stage is a common-source amplifier with its source connected to Vss and its drain connected to the gates of the third stage and a load resistor $R4$. The third stage is a common-source amplifier with its source connected to Vss and its drain connected to the output node, which is also connected to a load resistor $R2$ and a hold capacitor C_{hold} . The output is labeled $Output$. A control signal $Control$ is applied to the gates of DPT 1 and DPT 2 through a delay block $D1$. The delay block is implemented using a PMOS transistor and an inverter. The PMOS transistor's gate is connected to $Vdd1$ and its source to Vss . The inverter's input is connected to the $Control$ signal and its output to the gates of DPT 1 and DPT 2. The PMOS transistor's gate is also connected to the inverter's input. The PMOS transistor is labeled $D1$ and the inverter is labeled $Inverter$. The PMOS transistor's gate is connected to $Vdd1$ and its source to Vss . The inverter's input is connected to the $Control$ signal and its output to the gates of DPT 1 and DPT 2. The PMOS transistor's gate is also connected to the inverter's input.

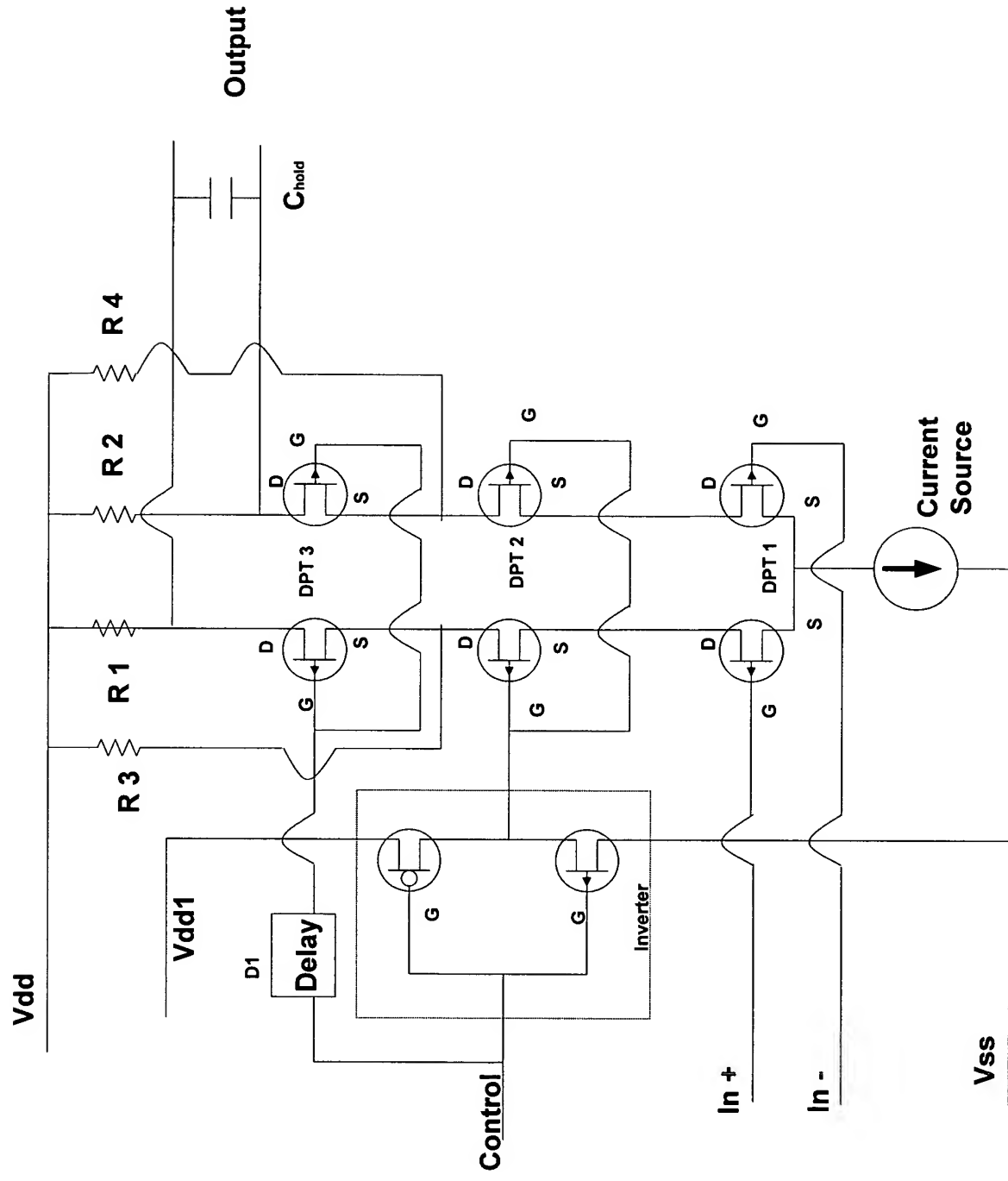


FIGURE 6

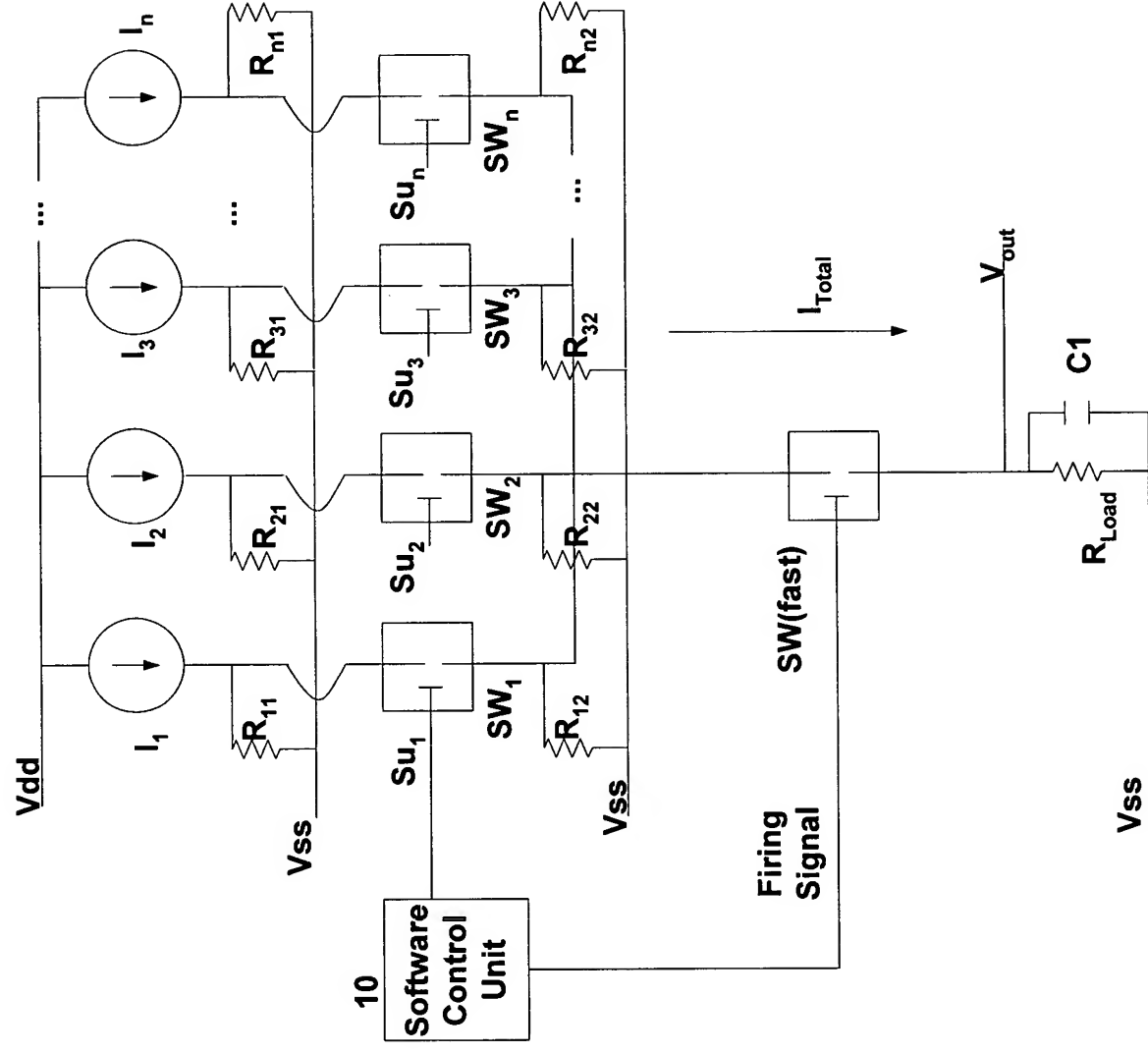


FIGURE 7

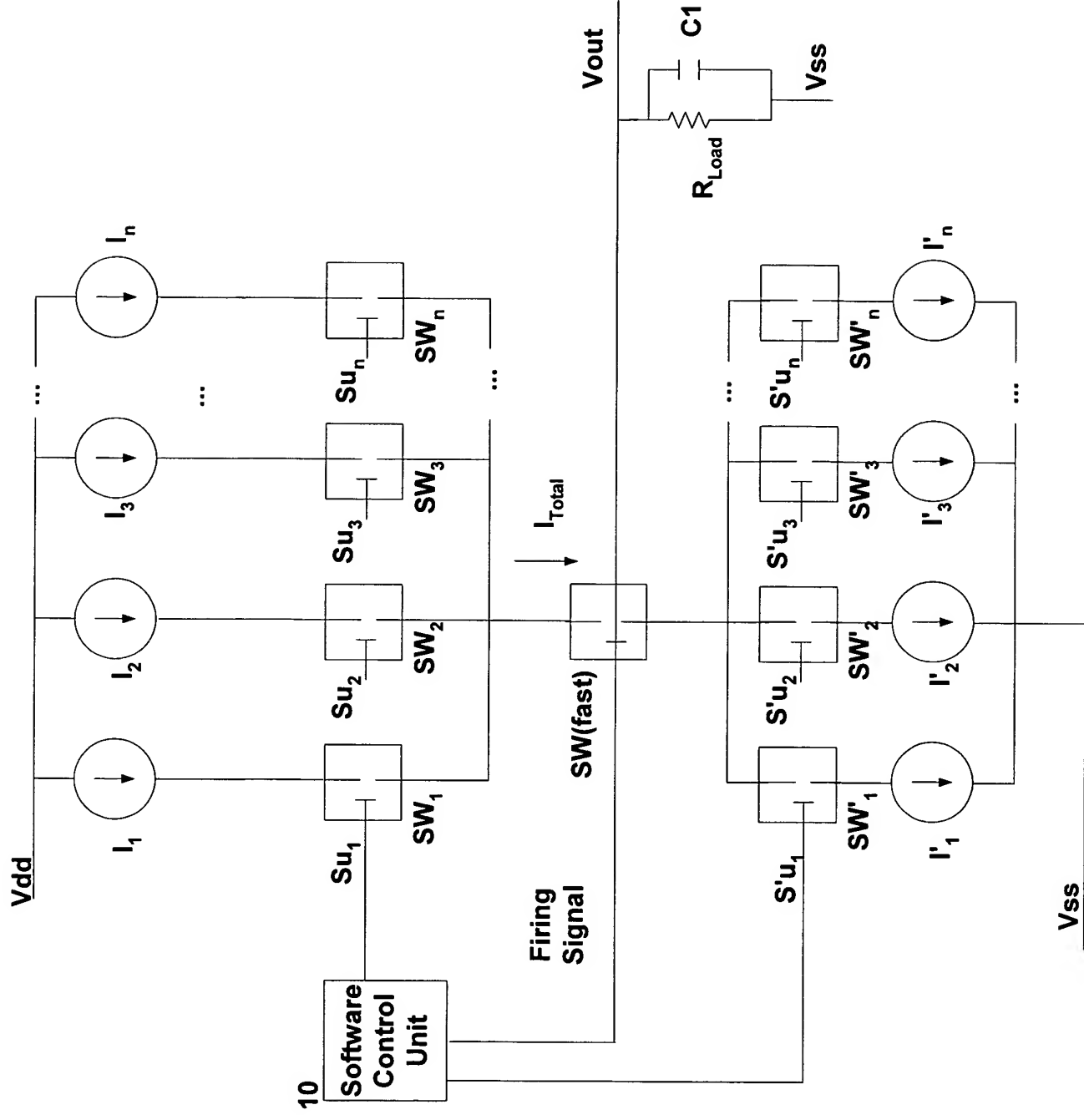


FIGURE 8

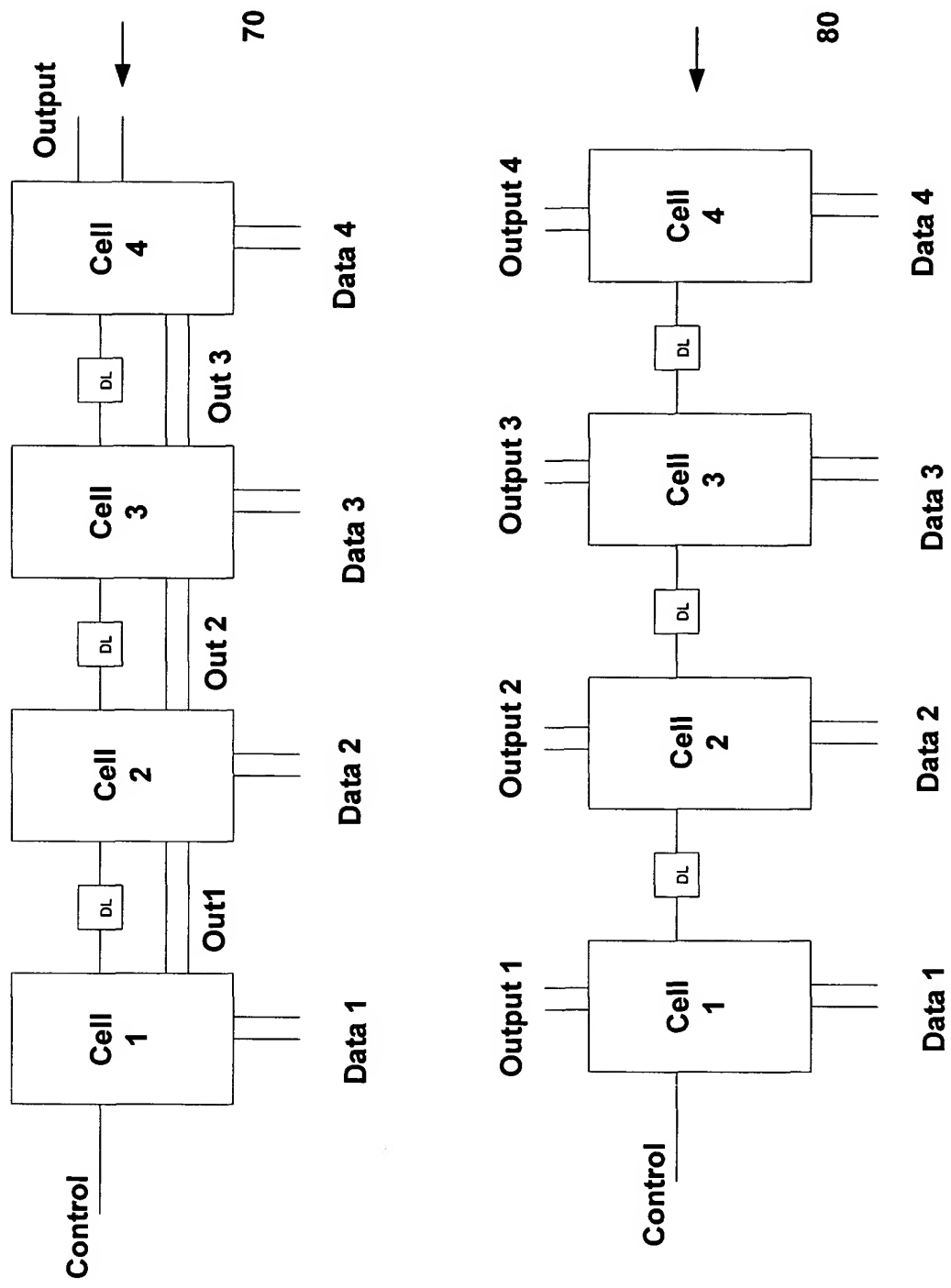


FIGURE 9

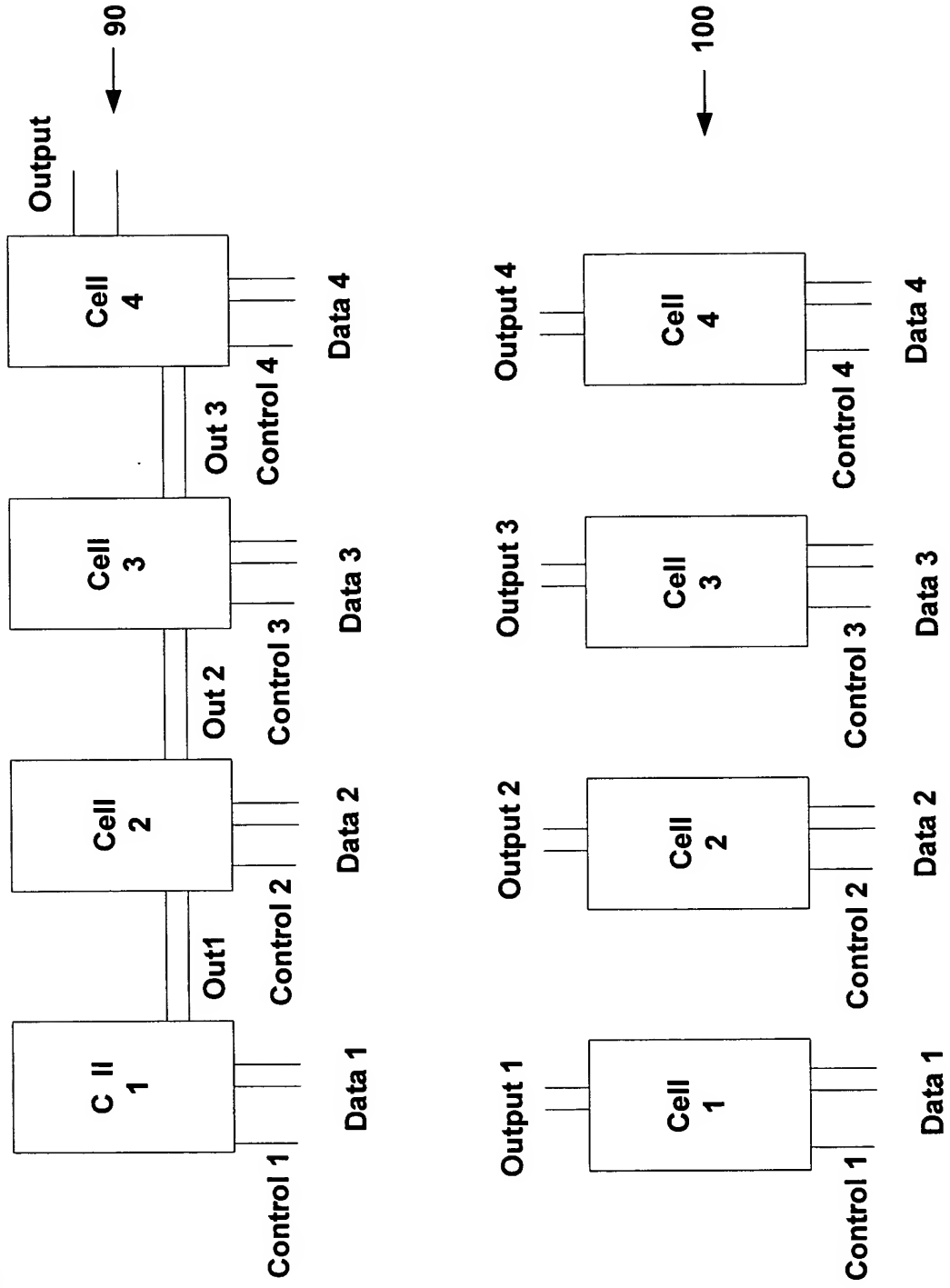


FIGURE 10

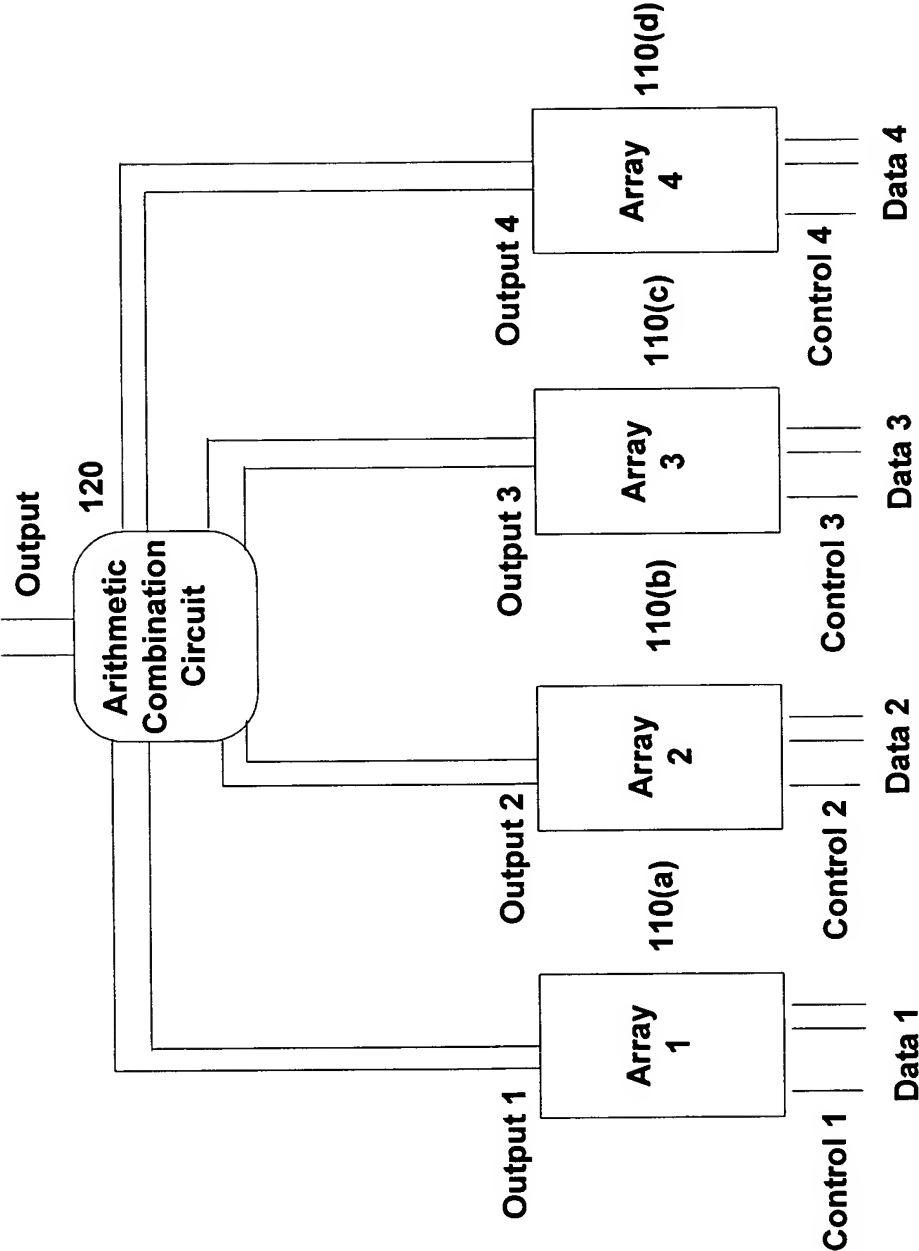


FIGURE 11

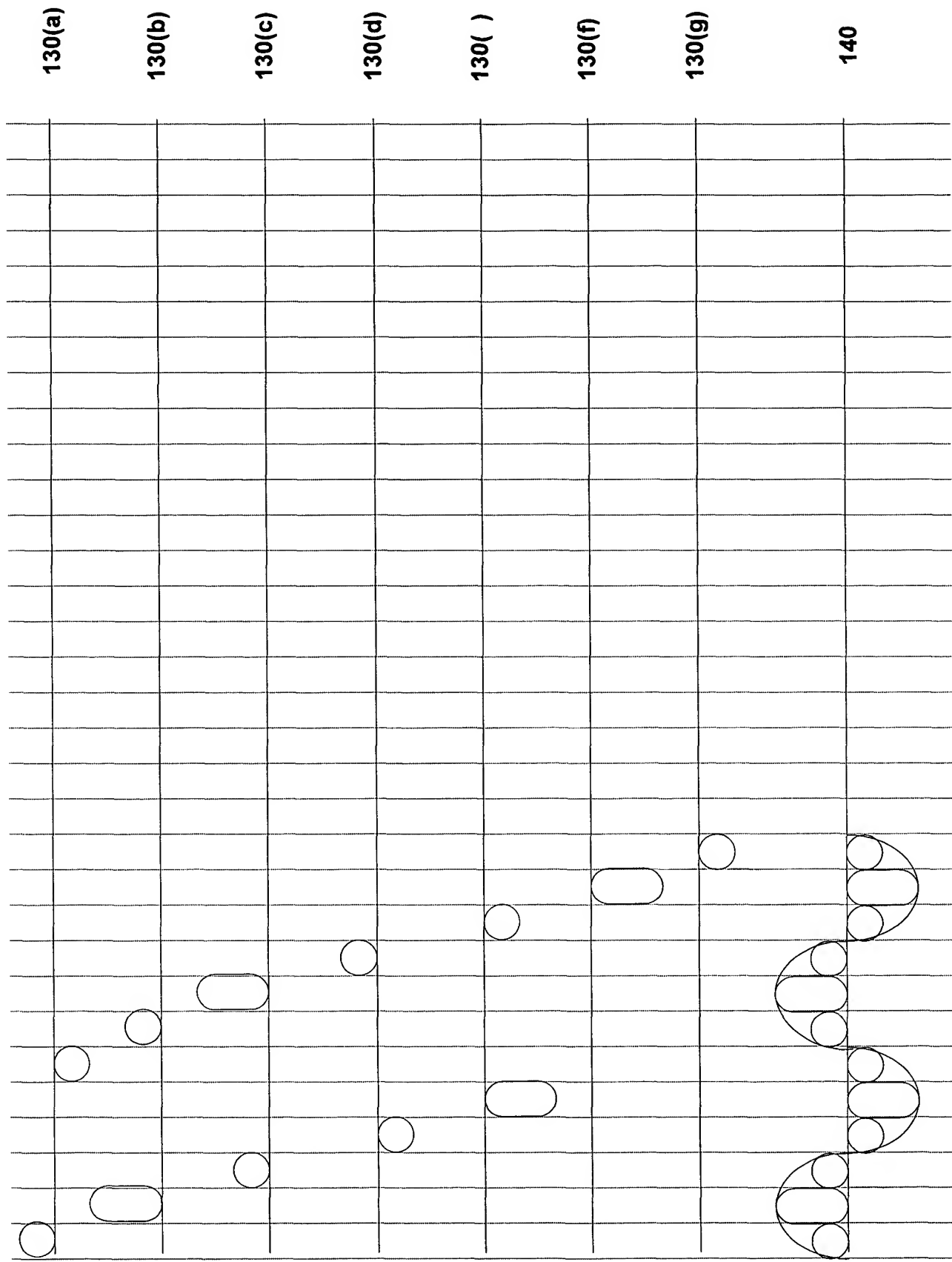


FIGURE 12

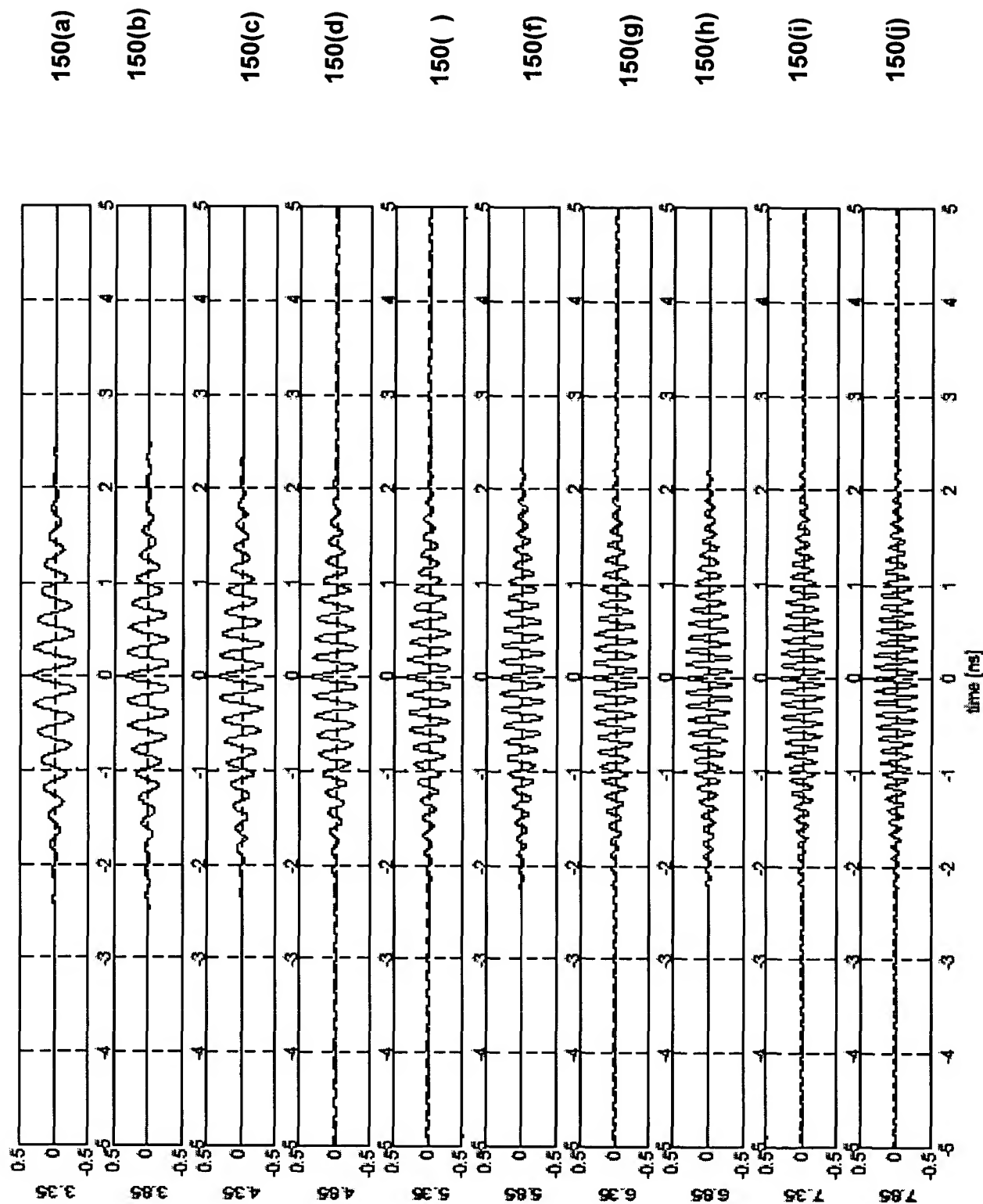


FIGURE 13

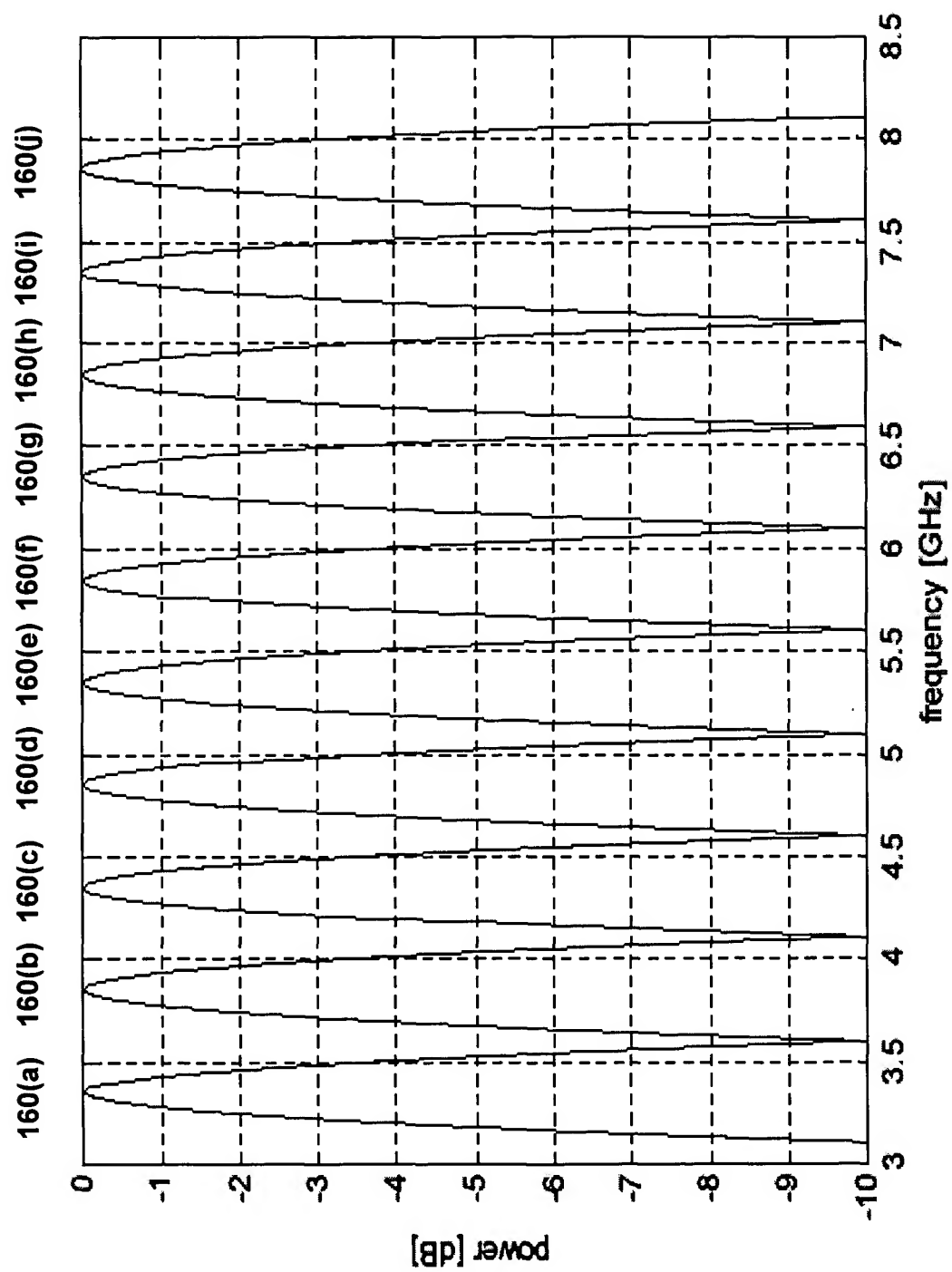


FIGURE 14

$\longleftrightarrow T_0$

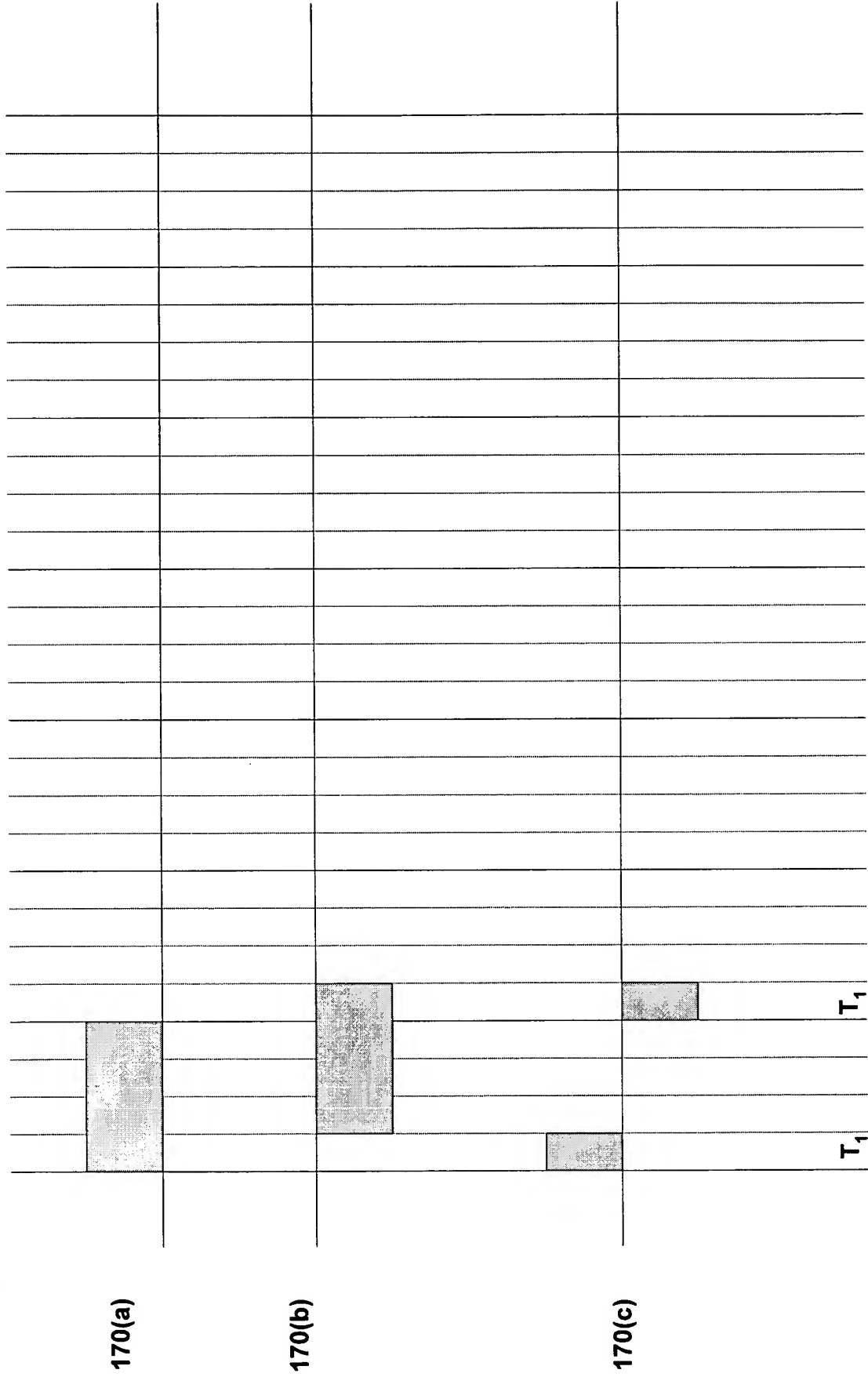


FIGURE 15

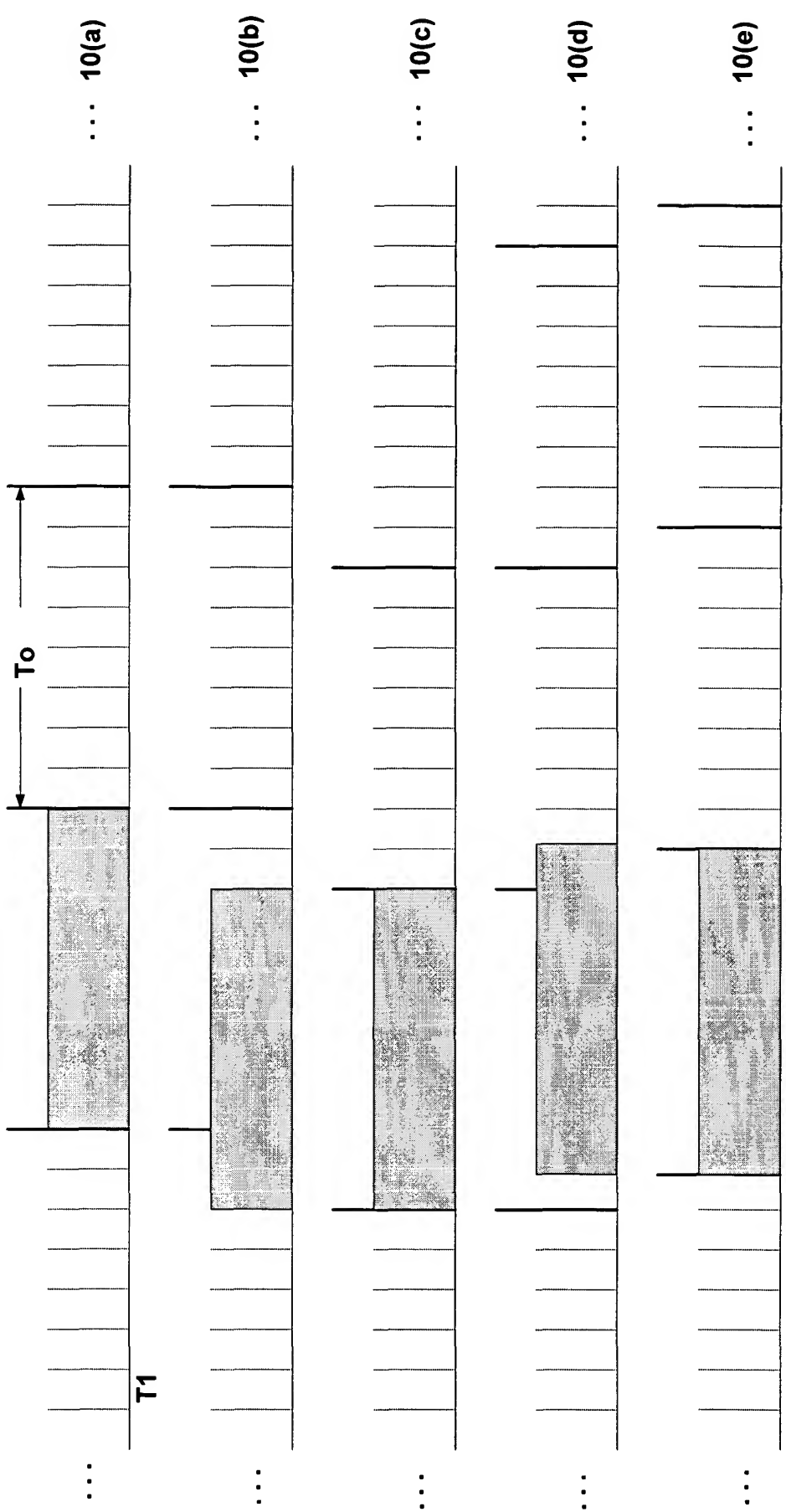


FIGURE 16

